REMARKS

In response to the rejections made on Claims 1-10 under U.S.C 102(e) as being anticipated by U.S Patent No. 6,691,219 B2 Ma et al. the applicant has provided the following response:

The rejection of Claim 1 on Ma et al. under 35 U.S.C. 102(e)

In regards to the rejection of claim 1, the Examiner states that Ma et al. teaches " a method that extends the addressing capability of an 8-bit micro-controller to memory space up to 16M capacity". Please note that the applicant asserts in claim 1 a method in which internal (strong emphasis) memory in a processor can be increased. The reference used by the examiner suggests extending the addressing capability referring to the memory registers outside of the micro-controller core. Ma et al. teaches that his design " allows for up to 16M of program memory and 16M of data memory" [Col2 20-25]. Program memory and data are typically not stored in internal memory because the internal memory is reserved for accessing data that is frequently utilized or requires fast access, such as internal register data or stack data.

Additionally, claim 1 is amended to include additional limitations regarding the inclusion of a conventional internal memory, the inclusion and operation of the extended internal memory as a stack, and their relative location within a memory block. These amendments are fully supported by the original disclosure as filed, and no new matter is added. These amendments are considered by the applicant to more accurately define the scope of the subject matter that the inventors consider their invention.

In the claimed invention, it is still possible to access the original conventional

internal memory as a stack, wherein the conventional internal memory is used as the default stack location (ie. can access the stack with an 8 bit SP). This is in contrast to Ma et al. who teaches that an extra 1K internal RAM is used for the stack location instead(emphasis added) of the original conventional internal memory [Fig. 5B, Col 18 5-10]. Ma et al. teaches "when the SA bit is set to a logic 1, the stack is addressed using a 10-bit SP, and is operated in the 1K internal RAM". Therefore, the claimed invention can still access extended internal memory in an 8 bit SP mode, whereas Ma et al. uses a 10 bit SP mode.

The claimed invention further provides a method to access the extended internal memory as a stack with the number of address bits being larger than the data width of the command set. For example, a traditional processor with an 8 bit command is limited to access a stack memory of 256 bytes. If the processor needs to access a larger memory array, the bit length of command set can be increased more than 8 bits. Alternatively, two (or more) commands can be used as the address of the internal memory. In this situation the memory addresses have a bit width of 16 bits(or more). The memory array can now comprise up to 64K bytes. If only 10 bits are used for memory addressing of the 16 bits in the 2 command width case, it can access 1K memory according to Ma et al.

An alternative method is provided by the claimed invention than that prescribed by Ma et al. The present invention utilizes the stacks push and pop functions to access memory, allowing an 8 bit processor to use only one command width to access internal memory addresses, and can access the extended internal memory as stack.

The claimed invention still requires the processor to initialize the stack pointer under 256 bytes, however, through the use of push(or pop) commands, this invention provides a way to access the extended internal memory as stack, wherein the extended internal memory is beyond the 256 bytes of conventional internal memory.

Furthermore, in regards to the original conventional internal memory initially used for the program stack, Ma states "the 256 bytes of Program Stack memory in the Scratchpad can be used as additional memory space" [Col 18, 12-15] when in extended mode. Therefore, the invention of Ma must require another memory space for stack operation in extended mode, and does not readily utilize the original stack memory location. This is in contrast to the claimed invention, which maintains use of the original conventional memory as a stack location regardless of the use of extended stack mode. The invention by Ma et al. occupies two different stack memory locations through the two different modes. One is the original 256 byte location in the 8 bit addressing(SP) mode, and the other is the 1K byte location for the 10 bit addressing mode(SP+ESP). The present invention however only occupies one stack location.

In Summary, the present invention allows for the conventional internal memory to be maintained and utilized as the default stack location while providing expanded stack memory, whereas the teachings of Ma et al. relocate the stack location to an external RAM source and rely on an bit generator to expand stack memory.

Based upon the structural differences of the two inventions above, the applicant kindly requests that the Examiner re-evaluate the amended claim and allow for its acceptance.

The rejection of Claims 2-10 on Ma et al. under 35 U.S.C. 102(e)

Regarding the rejections of Claims 2-10, please note that these claims are dependant on the currently amended independent Claim 1. Therefore, if Claim 1 is allowed, applicant asserts that Claims 2-10 be allowed as well as they are dependant on the mother

claim.

The withdrawal of Claim 6

Please note that original Claim 6 has now been withdrawn, as the key concept of this claim was integrated into the newly amended claim 1 to more accurately define the scope of the invention.

The amendment of Claims 7, 8, and 9

These claims were simply amended to more accurately reflect the terminology and description of terms used in newly amended claim1. No additional subject matter was introduced through the amendment of these claims.

The introduction of new Claims 11-16

To further highlight the uniqueness and novelties associated with the present invention, the applicant has introduced the above mentioned claims.

In regards to Claim 11, the applicant teaches setting the initial starting location of the stack pointer to the ending address of conventional internal memory. This is not shown in the teachings of Ma et al., who mentions the possibility of a stack overflow " from FFh to 00h"[Col 18 20-25]. This insinuates that the default starting location in the teachings of Ma et al. is set at 00h, and thus not at the ending address of conventional internal memory.

In regards to Claim 12, the applicant asserts that Ma et al. does not teach the inclusion of two stack pointers, one for pointing to a first stack, and a second for pointing to a second stack. Figure 5B of Ma et al. show an alternate configuration in extended

stack pointer mode, where an "8-bit stack pointer register is extended by an extended stack pointer register... can address at least 1K bytes of Program Stack memory within the data memory" [Col 18 1-10]. This is in contrast to the present invention, where a dual stack pointer configuration is used within the conventional internal memory.

In regards to Claim 13, applicant points out that Ma et al. does not teach the increasing the address of the stack pointer when data is added to the first stack, and decreasing the address of the second stack pointer when data is added to the second stack. This is shown in Figure 5 of the present invention, and is configured such that the two stacks cannot overlay or overwrite each other.

In regards to Claims 14-16, these claims discuss the usage and initialization of the two independent stack pointers. Again, this is not stressed by Ma et al. as a dual stack pointer configuration is not taught, and the initialization of the stack pointer at the ending address of conventional internal memory is not taught [Col 18 20-25].

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: OCT. 28, 2005

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

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